WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate;

a ferroelectric capacitor having a lower electrode, a ferroelectric film and an upper electrode which are stacked on said insulating film;

a first hydrogen barrier film

a first inter-layer insulating film covering said ferroelectric capacitor; and

a second inter-layer insulating film stacked on said first inter-layer insulating film,

said first hydrogen barrier film being interposed between said first and second interlayer insulating films.

2. The semiconductor device according to claim 1 wherein said first inter-layer insulating film has a thickness limited in the range of not smaller than 0.05 times to not larger than three times of the thickness of said ferroelectric capacitor.

3. The semiconductor device according to claim 1 wherein said first inter-layer insulating film contains a silicon oxide or a silicon nitride as a major component thereof.

4. The semiconductor device according to claim 1 wherein said first insulating film is formed at a temperature not higher than 400°C.

5. The semiconductor device according to claim 1 wherein said first and second inter-layer insulating films are made of a material different from that of said first hydrogen barrier film.

6. The semiconductor device according to claim 1 wherein said first hydrogen barrier film is made of a metal oxide which has a hydrogen diffusion constant not higher than 10^{-5} cm^2/s in its interior portion.

7. The semiconductor device according to claim 1 wherein said first hydrogen barrier film is made of a metal oxide whose specific resistance is not smaller than 1kΩcm.

8. The semiconductor device according to claim 1 wherein said hydrogen barrier film contains at least one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, Ti_xO_y, Zr_xO_y, Mg_xO_y and $Mg_xTi_yO_z$ as a major component thereof.

9. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate;

a ferroelectric capacitor having a lower electrode, a ferroelectric film and an upper electrode; and

a first hydrogen barrier film,

wherein said ferroelectric capacitor is buried in a groove formed in said insulating film, and said first hydrogen barrier film is provided inside said groove to cover at least the bottom surface and side surfaces of said ferroelectric capacitor.

10. The semiconductor device according to claim 9 further comprising a second hydrogen barrier film provided on said ferroelectric capacitor and not containing titanium.

11. The semiconductor device according to claim 9 wherein said first hydrogen barrier film is made of a metal oxide whose specific resistance is not smaller than 1kΩcm.

12. The semiconductor device according to claim 9 wherein said first hydrogen barrier film contains at least one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, Zr_xO_y and Mg_xO_y as a major component thereof.

13. The semiconductor device according to claim 10 wherein said second hydrogen barrier film contains at least one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, Zr_xO_y and Mg_xO_y as

a major component thereof.

14. The semiconductor device according to claim 9 further comprising an inter-layer insulating film interposed between said first hydrogen barrier film and said capacitor.

15. The semiconductor device according to claim 14 wherein said inter-layer insulating film contains a silicon oxide or a silicon nitride as a major component thereof.

16. The semiconductor device according to claim 14 wherein said first hydrogen barrier film contains at least one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, Ti_xO_y, Zr_xO_y, Mg_xO_y and $Mg_xTi_yO_z$ as a major component thereof.

17. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on said semiconductor substrate;

a ferroelectric capacitor having a lower electrode, a ferroelectric film and an upper electrode which are stacked sequentially on said insulating film; and

a first hydrogen barrier film not containing titanium.

18. The semiconductor device according to claim 17 wherein said first hydrogen barrier film is made of a metal oxide which has a hydrogen diffusion constant not higher than 10^{-5} cm^2/s in its interior portion.

19. The semiconductor device according to claim 17 wherein said first hydrogen barrier film is interposed between said lower electrode and said insulating film.

20. The semiconductor device according to claim 19 wherein a re-deposit film containing the material of the hydrogen barrier film and formed on side surfaces of said ferroelectric film and said lower electrode.

21. The semiconductor device according to claim 19 wherein said hydrogen barrier film contains at leas one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, AlN, WN, $SrRuO_3$, Ir_xO_y, Zr_xO_y, Ru_xO_y, Sr_xO_y, Re_xO_y, Os_xO_y and Mg_xO_y as a major component thereof.

22. The semiconductor device according to claim 17 wherein said first hydrogen barrier film is provided on said upper electrode.

23. The semiconductor device according to claim 22 wherein said hydrogen barrier film contains at leas one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, AlN, WN, $SrRuO_3$, Ir_xO_y, Zr_xO_y, Ru_xO_y, Sr_xO_y, Re_xO_y, Os_xO_y and Mg_xO_y as a major component thereof.

24. The semiconductor device according to claim 17 wherein said ferroelectric film and said lower electrode have a larger area than said upper electrode, and said first hydrogen barrier film extends at least from the upper surface of said upper electrode through side surfaces thereof onto the surface of said ferroelectric film extending beyond perimeters of said upper electrode.

25. The semiconductor device according to claim 24 wherein said first hydrogen barrier film is made of a metal oxide whose specific resistance is not smaller than 1kΩcm.

26. The semiconductor device according to claim 24 wherein said hydrogen barrier film contains at least one selected from the group consisting of Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, Zr_xO_y and Mg_xO_y as a major component thereof.

27. The semiconductor device according to claim 17 wherein said lower electrode has a larger area than said upper electrode and said ferroelectric film, and said first hydrogen barrier film extends from the upper surface of said upper electrode through side surfaces thereof and side surfaces of said ferroelectric film onto the surface of said lower electrode extending beyond perimeters of said ferroelectric film.

28. The semiconductor device according to claim 27 wherein said first hydrogen barrier film is made of a metal oxide whose specific resistance is not smaller than 1kΩcm.

29. The semiconductor device according to claim 27 wherein said hydrogen barrier film contains at least one selected from the group consisting of Al_xO_y, $Al_xSi_yO_z$, Zr_xO_y and Mg_xO_y as a major component thereof.

30. The semiconductor device according to claim 17 further comprising:

a first $Sr_xRu_yO_z$ film provided between said ferroelectric film and said lower electrode; and

a second $Sr_xRu_yO_z$ film provided between said ferroelectric film and said upper electrode,

said first and second $Sr_xRu_yO_z$ films having thickness $T_{sro}(BE)$ (nm) and $T_{sro}(TE)$ (nm) which are limited in the range of $10 \leq T_{sro}(BE)+T_{sro}(TE) \leq (2/12)T_{pzt}$ with respect to the thickness T_{pzt} (nm) of said ferroelectric film.

31. The semiconductor device according to claim 17 further comprising:

a titanium compound film formed on said upper electrode;

an inter-layer insulating film provided on said titanium compound film; and

a wiring connected to said upper electrode through a contact hole formed through said inter-layer insulating film.

32. The semiconductor device according to claim 31 wherein said wiring is an aluminum reflow wiring.

33. A semiconductor device comprising:

a semiconductor substrate;

a transistor formed on said semiconductor substrate;

an insulating film covering said semiconductor substrate and said transistor;

a contact plug buried in said insulating film and connected to a diffusion layer of said transistor; and

a ferroelectric capacitor formed on said insulating film and connected to said transistor by said contact plug,

said ferroelectric capacitor having a lower electrode, a ferroelectric film formed on said lower electrode, an upper electrode formed on and having an area smaller than said ferroelectric film, and a protective film formed in self alignment with side walls of said upper electrode to cover the surface of said ferroelectric film.

34. A semiconductor device comprising:

a semiconductor substrate;

an insulating film made on said semiconductor substrate;

a ferroelectric capacitor having a lower electrode, a ferroelectric film and an upper electrode which are stacked sequentially on said insulating film;

an inter-layer insulating film provided on said capacitor; and

a wiring connected to said upper electrode through a contact hole made through said inter-layer insulating film,

said wiring having a contact area to said upper electrode which occupies not less than 50% of the area of the upper surface of said upper electrode.

35. The semiconductor device according to claim 34 further comprising a transistor formed on said semiconductor substrate,

said wiring having a contact to said transistor, and said wiring having a contact area to said upper electrode which is larger than a contact area thereof to said transistor.

36. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming a first hydrogen barrier film not containing titanium on said insulating film;

sequentially stacking a lower electrode material film, a

ferroelectric film and an upper electrode material film on said first hydrogen barrier film;

etching said upper electrode material film by using a first mask to pattern an upper electrode; and

sequentially etching said ferroelectric film and said lower electrode material film by using a second mask covering said upper electrode to pattern the ferroelectric film and a lower electrode self-aligned therewith.

37. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

sequentially forming a lower electrode material film, a ferroelectric film and an upper electrode material film on said insulating film;

stacking a hydrogen barrier film not containing titanium on said upper electrode material film;

sequentially etching said hydrogen barrier film and said upper electrode material film by using a first mask to pattern an upper electrode; and

sequentially etching said ferroelectric film and said lower electrode material film by using a second mask covering the region of said upper electrode to pattern the ferroelectric film and a lower electrode self-aligned therewith.

38. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

sequentially forming a lower electrode material film, a ferroelectric film and an upper electrode material film on said insulating film;

etching said upper electrode material film by using a first mask to pattern an upper electrode;

stacking a hydrogen barrier film not containing titanium on said upper electrode and exposed part of said ferroelectric film;

sequentially etching said ferroelectric film and said

lower electrode material film by using a second mask formed on said hydrogen barrier film to cover the region of said upper electrode so as to pattern the ferroelectric film and a lower electrode self-aligned therewith.

39. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

sequentially forming a lower electrode material film, a ferroelectric film, an upper electrode material film and a hydrogen barrier film not containing titanium on said insulating film;

forming and patterning a silicon nitride film mask on said hydrogen barrier film;

etching said hydrogen barrier film and said upper electrode material film by using said silicon nitride film mask to pattern an upper electrode;

patterning said ferroelectric film and said lower electrode material film so that they have a larger area than said upper electrode, and thereby making a ferroelectric capacitor; and

stacking an inter-layer insulating film covering said ferroelectric capacitor, and leveling said inter-layer insulating film by a polishing process using said silicon nitride film as a stopper.

40. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

sequentially stacking a lower electrode material film, a ferroelectric film and an upper electrode material film on said insulating film;

sequentially etching said upper electrode material film and said ferroelectric film by using a first mask to pattern an upper electrode and the ferroelectric film self-aligned with said upper electrode;

removing said first mask, and stacking a hydrogen barrier

film not containing titanium on said upper electrode and exposed part of said lower electrode material film; and

etching said hydrogen barrier film and said lower electrode material film by using a second mask formed on said hydrogen barrier film to cover the region of said upper electrode so as to pattern a lower electrode.

41. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming a groove in a capacitor region of said insulating film;

forming a hydrogen barrier film non containing titanium in said groove; and

forming a ferroelectric capacitor buried inside said groove, said ferroelectric capacitor having a multi-layered structure including a lower electrode, a ferroelectric film and an upper electrode, and a bottom surface and side surfaces thereof being protected by said hydrogen barrier film.

42. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

forming a ferroelectric capacitor having a multi-layered structure including a lower electrode, a ferroelectric film and an upper electrode on said insulating film;

forming a first inter-layer insulating film covering said ferroelectric capacitor;

forming a hydrogen barrier film on said first inter-layer insulating film, said hydrogen barrier layer preventing diffusion of hydrogen into said ferroelectric capacitor;

forming a second inter-layer insulating film on said hydrogen barrier film; and

forming on said hydrogen barrier film a wiring to be connected to said ferroelectric capacitor.

43. The method for manufacturing a semiconductor device

according to claim 42 wherein said first insulating film is formed at a temperature not higher than 400°C.

44. A method for manufacturing a semiconductor device comprising the steps of:

forming an insulating film on a semiconductor substrate;

sequentially stacking a hydrogen barrier film not containing titanium, a lower electrode material film, a ferroelectric film and an upper electrode film on said insulating film;

etching said upper electrode material film by using a first mask to pattern an upper electrode;

forming a second mask covering said upper electrode, and sequentially dry-etching said ferroelectric film, said upper electrode material film and said hydrogen barrier film to pattern said ferroelectric capacitor and a lower electrode in alignment therewith, and simultaneously therewith, forming a re-deposit film containing the material of said hydrogen barrier film on side surfaces of said lower electrode and said ferroelectric film.

45. A method for manufacturing a semiconductor device comprising the steps of:

making a transistor on a semiconductor substrate;

forming an insulating film on said semiconductor substrate having formed said transistor;

burying a contact plug connected to a diffusion layer of said transistor into said insulating film;

sequentially stacking a lower electrode material film, a ferroelectric film and an upper electrode material film on said insulating film;

etching said upper electrode material film by using a hard mask formed on said upper electrode material film to pattern an upper electrode;

forming a protective film in self-alignment with said hard mask and side walls of said upper electrode; and

etching said ferroelectric film and said lower electrode material film by using said hard mask and said protective film

as a mask, and thereby patterning the ferroelectric film and a lower electrode in self alignment therewith.

46. A method for manufacturing a semiconductor device comprising the steps of:

making an insulating film on a semiconductor substrate;

making a ferroelectric capacitor on said insulating film, said ferroelectric capacitor having a multi-layered structure including a lower electrode, a ferroelectric film and an upper electrode;

making a first inter-layer insulating film covering said ferroelectric capacitor;

making a hydrogen barrier film on said first inter-layer insulating film, said hydrogen barrier film preventing diffusion of hydrogen into said ferroelectric capacitor;

making a second inter-layer insulating film on said hydrogen barrier film;

making a wiring on said second inter-layer insulating film to be connected to said ferroelectric capacitor; and

removing a part of said second inter-layer insulating film by etching to make a wiring groove therein,

said hydrogen barrier film being used as an etching stopper in said step of making the wiring groove.

47. The manufacturing method of a semiconductor device according to claim 46 wherein a film made by stacking Si_xN_y or $Si_xO_yN_z$ on said hydrogen barrier film is used as a stopper during CMP.